Listing of the Claims

Claims 1-15 (canceled)

Claim 16. (new)

A method of interfacing for the transfer of data in variable length packets and cells, and control information, wherein the transfer takes place between a first layer device and a second layer device over a first physical path and a second physical path, and wherein the control information comprises a plurality of control words, said method comprising the steps of:

Step (a) dividing the control information into an in-band portion and an out-of-band portion;

Step (b) transmitting the in-band portion of the control information and the data along the first physical path from one of the first and second layer devices to the other of the first and second layer devices, wherein the in-band portion control information controls data bus lanes and not data, and wherein the in-band portion of the control information comprises:

i. status information;

ii. a destination address for the data; and,

iii. information required to insure alignment of data and control information transmitted along the first and second physical paths from one of the first and second layer devices to the other;

Step (c) inserting a control of data signal into the first physical path of Step (b), wherein the data signal identifies when the path contains the control information and when it contains the data;

Step (d) transmitting the out-of-band portion of the control information of Step (a) along the second physical path, wherein the out-of-band portion comprises credit-based first-in-first-out (FIFO) status flow information; and,

Step (e) granting a number of credits to one or more ports, wherein the number of credits granted depends on a state of a corresponding port status;

wherein transmission occurs independently in both transmit and receive directions, whereby re-encoding of data and insertion of control information upon pre-determined intervals is avoided.

Claim 17. (new)

A method according to Claim 16, further comprising the step of marking boundaries of a framing pattern with a "1 1" pattern on a FIFO status channel, wherein an out-of-band framing signal is not required.

Claim 18. (new)

A method according to claim 16, further comprising the steps of:

Step (f) sending a training control pattern periodically to a receive interface; and,

Step (g) using the training control pattern sent by Step (f) to check and correct for skew variations.

Claim 19. (new)

A method according to Claim 18, wherein the data and the control information of the in-band portion of Step (b) are aligned according to a source-synchronous clock, and wherein the data, the control information, and the training control pattern are

transmitted at intervals that are configurable on start-up.

Claim 20. (new)
A method according to Claim 16, further comprising the step of transmitting a clock signal in a direction opposite to the transmitting direction of Step (b).

Claim 21. (new)
A method according to Claim 16, further comprising the step of inserting at least one control word between bounded transfer periods for transfer of packets or portions thereof, wherein the control word comprises an error-detection code, whereby performance of the error detection code is not degraded by transfers.

Claim 22. (new)
A method according to Claim 16, further comprising the step of combining an end-of-packet event and at least one error code into a two-bit code.

Claim 23. (new)
A method according to Claim 16, wherein the control information of at least one control word applies to i) data preceding the one control word, and, ii) data following the one control word.

Claim 24. (new)
A method according to Claim 16, wherein the first layer device is a physical layer (PHY) device, and wherein the second layer device is a link layer device.

Claim 25. (new)

A method according to claim 16, wherein:

i. the in-band portion of the control information includes packet address, delineation, and error control coding;

ii. the out-of-band portion of the control information comprises FIFO status flow information; and,

iii. an interface between the first layer device and the second layer device operates independently in both transmit and receive directions.

Claim 26. (new)

A de-skewing circuit for de-skewing data arriving on M data lines, where M is an integer greater than zero, said de-skewing circuit comprising:

(a) M serial-in parallel-out (SIPO) blocks, wherein each of said SIPO blocks is coupled to a corresponding one of said data lines, and wherein said SIPO blocks convert M-bit words of serial input data from said data lines to parallel data;

(b) M register sets, wherein each of said register sets is coupled to one of said SIPO blocks, and wherein each of said register sets stores the most recent M-bit words of serial input data arriving on each of said data lines;

(c) a training detector block coupled to said register sets, wherein said training detector block detects the presence of a training pattern based on the contents of said register sets;

(d) a plurality of transition detection blocks, wherein each transition detection block is coupled to a respective one of said register sets, and wherein each of said transition

detection blocks searches for and detects a transition in each bit position within its respective register set; and,

(e) an aligner block coupled to said plurality of transition detection blocks, wherein said aligner block selects appropriate bits within each of said register sets from which to read each bit in order to present a de-skewed output.

Claim 27. (new)

The de-skewing circuit of Claim 26, wherein M is equal to 17.

Claim 28. (new)

A de-skewing circuit, comprising:

(a) N serial input data lines, wherein N is an integer greater than zero;

(b) N serial-in parallel-out (SIPO) blocks, wherein each of said SIPO blocks comprises an N-bit parallel output, and wherein each SIPO block is coupled to a respective one of said serial input data lines, whereby serial data transmitted to said SIPO blocks is converted to N-bit parallel output data comprising separate output for each bit of said N-bit parallel output data;

(c) N register sets, wherein each register set is coupled to a respective one of said SIPO blocks, and wherein each of said register sets stores the most recent n-bit words of data arriving on each of said input data lines;

(d) a training detector block coupled to outputs of said register sets, wherein said training detector block detects the presence of a training pattern based on the contents of said register sets;

(e) N transition detection blocks, wherein:

i. each of said transition blocks comprises N inputs;

ii. each of said inputs is coupled to an output of a respective one of said register sets; and,

iii. after the presence of the training pattern has been detected within said register sets by said training detection block, said transition detection blocks independently search for a transition of bits within the training pattern detected by said training detector block; and,

(f) an aligner block, wherein said aligner block is coupled to outputs from said transition detection blocks and to outputs of said register sets, and wherein said aligner block selects a register set from which to read each of N bits from the selected register set, whereby variable length packet and cell transfers are corrected for relative skew differences of up to plus or minus [+/-] 1 bit time.

Claim 29. (new)

The de-skewing circuit of Claim 28 wherein N is equal to 17.